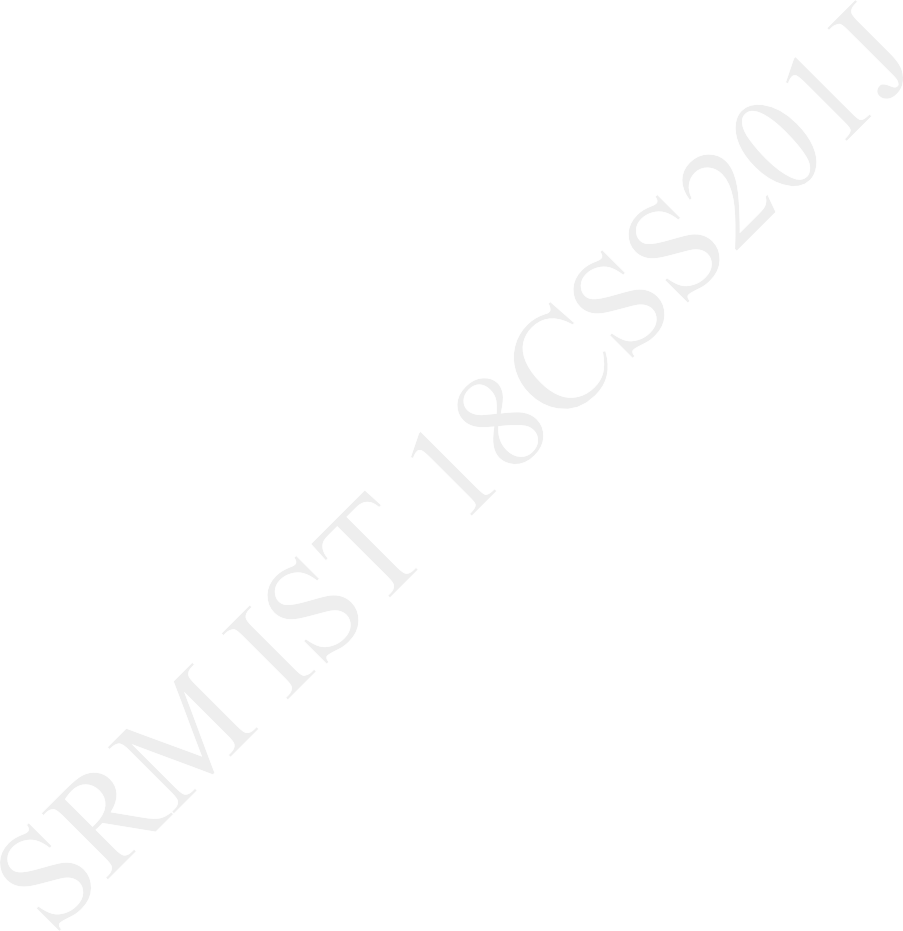
# ---Part – A

1. The logical expression Y=AB+AC+BC is known as
   1. Standard Sum of Product form
   2. Sum of Product form
   3. standard Product of Sum form
   4. Product of Sum form ANSWER: B
2. The number of cells in 6 variable K-map is
   1. 4
   2. 16
   3. 32
   4. 64 ANSWER: D
3. On a K-Map, grouping the 0s produces
   1. SoP expression
   2. PoS expression
   3. a don’t care condition
   4. AND-OR expression ANSWER: B
4. In K map, for M variable, cells are required.
   1. M
   2. 2M
   3. 22M
   4. M\*M ANSWER: B
5. In Boolean algebra XY+XY’ +X’Y is equal to
   1. X
   2. Y
   3. XY
   4. X+Y ANSWER: D
6. Simplified form of A + A’B +A’B’C +A’B’C’D is equal to
   1. A
   2. A+B
   3. A+B+C
   4. A+B+C+D ANSWER: D
7. The code used for labeling the cells of a K-map is
   1. 8-4-2-1 binary
   2. Hexadecimal



1. Grey
2. Octal Answer C
3. The Quine– McClusky method of minimization of a logic expression is a (i) graphical method (ii) algebraic method (iii) tabular method (iv) a computer-oriented algorithm The correct answers are
   1. (iii) and (iv)
   2. (ii) and (iv)
   3. (i) and (iii)
   4. (i) and (ii) Answer: A
4. In simplification of a Boolean function of n variables, a group of 2m adjacent 1s leads to a term with
   1. m – 1 literals less than the total number of variables
   2. m + 1 literals less than the total number of variables
   3. n + m literals
   4. n – m literals Answer: D
5. Which one of the following devices has a greater number of inputs than outputs?
   1. encoder
   2. decoder
   3. multiplexer
   4. demultiplexer Ans: (c)
6. What is the number of selection lines required in a single input, n-output demultiplexer?
   1. 2
   2. n
   3. 2^n
   4. log(base-2) n Ans: (d)
7. A 1-to-8 demultiplexer has select input lines.
   1. 2
   2. 3
   3. 8
   4. 4 Ans: (b)
8. A 32 to 1 multiplexer has the following terminals
   1. 32 outputs, one input and 5 control signals
   2. 32 inputs, one output and 5 control signals
   3. 5 inputs, one control signal and 32 outputs
   4. 5 inputs 32 control signals and one output Ans:(b)
9. The following switching function is to be implemented using multiplexer f = ∑m(1, 2, 4, 8,14, 45). What is the size of multiplexer?
   1. 8-to-1 line
   2. 16-to-1 line
   3. 32-to-1 line
   4. 64-to-1 line Ans: (d)
10. In 16:4 priority encoder, highest priority is given on
    1. A
    2. 0
    3. 9
    4. F Ans: (d)
11. The following switching function is to be implemented using decoder. f = ∑m(1, 2, 4, 8, 14). What is the size of decoder?
    1. 2-to-4 line
    2. 3-to-8 line
    3. 4-to-16 line
    4. 5-to-32 line Ans: (c)
12. Size of decoder needed to design 16-to-1 line multiplexer.
    1. 2-to-4 line decoder
    2. 3-to-8 line decoder
    3. 4-to-16 line decoder
    4. 5-to-32 line decoder Ans: (c)
13. ABCD decoder has
    1. Four input lines and 16 output lines
    2. Four selection lines, one input line and 16 output lines
    3. Sixteen input lines and four output lines
    4. Four input lines and ten output lines Ans: (a)
14. Full adder circuit adds number of bits at a time
15. 5
16. 2
17. 5
18. 3 ANSWER :D
19. The Half adder circuit is implemented by
20. Using one XOR and one AND gate
21. Using one XNOR and one OR gate
22. Using two XOR and one AND gate
23. Using two XNOR and one OR gate ANSWER :A
24. How many full adder required to design 4 -bit parallel adder ?
25. 2
26. 4
27. 5
28. 3 ANSWER :B
29. The half subtractor logical expression for borrow is
30. A XOR B
31. AB
32. A’B
33. A’B’ ANSWER : C
34. The carry propagation delay reduced by A)Carry look ahead adder
35. Full addrer
36. Full subtractor
37. 4 -bit parallel adder Answer: A
38. The output sum expression for carry look ahead adder is
39. Si = Pi + Ci
40. Si = Gi + Pi Ci
41. Si = Pi XOR Ci
42. Si = Gi XOR Pi Ci ANSWER: C
43. Decimal adder is also called as
44. Binary adder
45. 4 – bit parallel adder
46. Carry look ahead adder
47. BCD adder ANSWER: D
48. The carry output of the lower order stage is connected to the carry input of the next higher order stage will be
49. Ripple carry adder
50. full adder
51. Half adder
52. Decimal adder ANSWER : A
53. The carry of the 4-bit parallel adder is connected to 1 then the carry -output is
54. That carry-out will be LOW
55. That carry-out will be HIGH
56. A one will be added to the final result
57. The carry-out is ignored ANSWER: C
58. The four-bit parallel adder will perform subtraction by
59. Inverting the outputs
60. Inverting the carry-in
61. Inverting the second inputs
62. Inverting the carry-out ANSWER: C
63. In 4-bit full adder the carry propagation delay is
64. cumulative for each stage and limits the speed at which arithmetic operations are performed
65. normally not a consideration because the delays are usually in the nanosecond range
66. Decreases in direct ratio to the total number of full-adder stages
67. Increases in direct ratio to the total number of full-adder stages, but is not a factor in limiting the speed of arithmetic operations

ANSWER: A

1. In decimal adder,the decimal number 10 is represented as A) 10100000

B) 01010111

C) 00010000

D) 00101011 ANSWER: C

1. A three-digit decimal number of needs for illustration in the BCD format.
2. 3 bits
3. 6 bits
4. 12 bits
5. 24 bits ANSWER: C
6. In BCD adder A = 0101 and B = 1001. find the output Y. A. 1110

B. 0001 0100

C. 1111

D. 0000 1110 ANSWER :B

1. The expression for C3 in Carry Propagation–Look-Ahead Carry generator is

a. G2 + P2G1 + P2P1G0 + P2P1P0C0

1. G1 + P1G0 + P1P0C0
2. G0 + P0C0

d. G1 + P1 (G0 + P0C0)

Answer : A

1. In 2-bit magnitude comparator A1AO = 11 and B1BO = 01 then A< B will be
2. 0
3. 1
4. A
5. B ANSWER: A
6. Which one is a basic comparator?
7. XOR
8. XNOR
9. AND
10. NAND Answer: a
11. A circuit that compares two numbers and determine their magnitude is called
12. Height comparator
13. Size comparator
14. Comparator
15. Magnitude comparator Answer: d
16. If A = 1010 & B= 0101 then the comparator output is
17. a > b
18. a – b
19. a < b
20. a = b Answer : a
21. Data stored in ROM is
22. Non-volatile
23. Volatile
24. Secondary
25. Primary

Answer : a

1. EPROM can be erased by
2. Electric pulses
3. UV Light
4. Sound waves
5. Cannot be erased Answer : b
6. The fundamental building block of a CPU is
7. Memory block
8. Arithmetic and Logic unit block
9. Power Supply module
10. None of the above Answer : a
11. Total memory capacity of ROM is
12. 2n
13. 2n-1
14. 2n\*m
15. 2n+m

Answer : c

1. The description of circuit in VHDL refers to register transfers level
2. Structural description
3. Dataflow description
4. Hierarchical Description
5. Behavioral Description Answer : d
6. Behavioral descriptions use the keyword… followed by a list of procedural

assignment statements

1. always
2. reg
3. input
4. endmodule Answer : a
5. The most basic form of behavioral modeling in VHDL is
6. IF statements
7. Assignment statements
8. Loop statements
9. WAIT statements Answer : b
10. Which model in system modelling depicts the dynamic behaviour of the system ?
11. Context Model
12. Behavioral Model
13. Data Model
14. Object Model Answer : b

d) Programmable AND Logic Answer: c

1. PLA contains
   1. AND and OR arrays
   2. NAND and OR arrays
   3. NOT and AND arrays
   4. NOR and OR arrays Answer: a
2. PLA is used to implement
   1. A complex sequential circuit
   2. A simple sequential circuit
   3. A complex combinational circuit
   4. A simple combinational circuit Answer: c
3. If a PAL has been programmed once
   1. Its logic capacity is lost
   2. Its outputs are only active HIGH
   3. Its outputs are only active LOW
   4. It cannot be reprogrammed Answer: d
4. Simplify the Boolean expression: XY + X(Y+Z) + Y(Y+Z)
5. XY+Z
6. XZ
7. Y+XZ
8. Y ANSWER: C
9. A switching function f(A,B,C) = (A+B'+C) (A+B'+C') (A'+B'+C) can also be written as

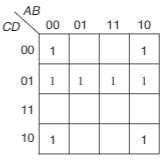
A. ∏(1,4,5)

B. ∏(2,4,6)

C. ∏(0,2,4)

D. ∏(3,4,5) ANSWER: A

1. The minimized expression for the given K-map is



1. B'CD' + B'C'D' +C'D
2. B'D' + C'D
3. A'BCD + AB'CD + ABC' + A'B'C'
4. C'D' + AB'C + A'BCD + AB'C ANSWER: B
5. The logical expression Y=∑m(0,4,6,7,10,11,14) is equivalent to A. ∏(0,3,6,7,10,12,15)

B. ∏(1,2,3,5,8,9,12,13,15)

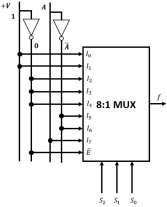
C. ∑(1,2,4,5,8,9,11,13,14)

D. ∑(0,2,4,6,8,10,12,14) ANSWER: B

1. What is the simplified form of the following Boolean function F=

∑(4,6,8,10,11,12,15) using K-map is

1. ACD+AB’D’+A’BD’
2. AC’D+A’CD’+AB’D’+A’BD’
3. AC’D’+ACD+AB’D’+A’BD’
4. AC’D+ACD+A’BD’+AB’CD’ ANSWER: C
5. In Boolean algebra XY+XY’ +X’Y is equal to
6. X
7. Y
8. XY
9. X+Y ANSWER: D
10. Simplified form of A + A’B +A’B’C +A’B’C’D is equal to
11. A
12. A+B
13. A+B+C
14. A+B+C+D ANSWER: D
15. Which one of the following Boolean function is correct for the given multiplexer circuit?



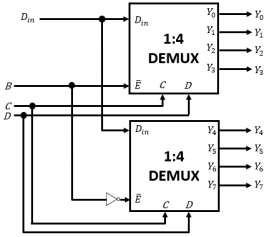
(a) f = ⅀m(0,1,3,4,8,9,15)

(b) f = ⅀m(2,3,4,7,10,11,12,13,14)

(c) f = ℿM(2,3,4,7,10,11,12,13,14)

(d) f = ℿM(2,5,6,7,10,11,12,13,14)

Ans: (c)

1. At which condition, the below demultiplexer circuit output Y3 and Y6 become 1? Verify with output function of Y3 and Y6.

(a) Din = 1, B = 0, C = 1, D = 1 and Din = 1, B = 1, C = 1, D = 1

(b) Din = 1, B = 1, C = 1, D = 1 and Din = 1, B = 0, C = 1, D = 1

(c) Din = 1, B = 0, C = 1, D = 0 and Din = 1, B = 1, C = 1, D = 1

(d) Din = 1, B = 0, C = 1, D = 1 and Din = 1, B = 1, C = 1, D = 0

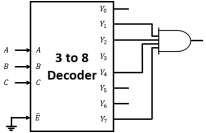
Ans: (d)

1. Which one of the following circuits is correct for the given truth table?

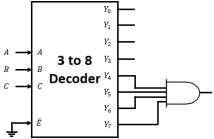
| A | B | C | Y |
| --- | --- | --- | --- |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |

| 0 | 1 | 0 | 1 |
| --- | --- | --- | --- |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

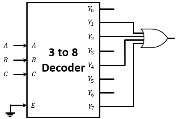
(a)



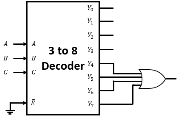
(b)



(c)



(d)



Ans: (c)

1. Which one of the following expressions is correct for hexa to binary encoder? (a) B3 = I4 + I5 + I6 + I7 + I8 + I9 + I10 + I11

(b) B2 = I2 + I3 + I4 + I5 + I10 + I11 + I12 + I13 (c) B1 = I2 + I3 + I6 + I7 + I10 + I11 + I14 +I15 (d) B0 = I1 + I3 + I5 + I6 + I8 + I10 + I12 + I14

Ans: (c)

63 Designed expression for carry of full adder is

1. AB + AC+ BC
2. AB + AC
3. A’ XOR B’ XOR c’
4. A XOR B XOR c ANSWER :A

64. In 4 – bit parallel adder A = 1011 and B = 0011. Find the 4-bit input carry. A) 0110

B) 0011 C)1010 D)1011 ANSWER: A

1. In two-bit magnitude comparator the logical expression for A > B is A) A1 B1’ + A0 B1’B0’ + A1 A0 BO’

B) A1’ B1 + A0’ B1B0’ + A1 A0’ BO’

C) A1 B1 + A0 B1B0 + A1 A0 BO

D) A1’ B1 + A0’ B1B0 + A1’ A’0 BO ANSWER: A

1. In two-bit magnitude comparator the logical expression for A < B is A) A1 B1’ + A0 B1’B0’ + A1 A0 BO’

B) A1’ B1 + A0’ B1B0’ + A1 A0’ BO’

C) A1 B1 + A0 B1B0 + A1 A0 BO

D) A1’ B1 + A0’ B1B0 + A1’ A’0 BO ANSWER: d

1. What logic circuit is described by the following code? ARCHITECTURE gate OF my\_gate IS

BEGIN

WITH ab SELECT

y<= 0 WHEN “01” OR “10”;

1 WHEN OTHERS;

END gate;

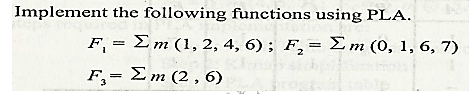
* 1. NAND
  2. NOR
  3. EXOR
  4. EXNOR Answer : d

# Part – B (4 marks)

1. What is a half order? Write its truth table
2. What is a full order
3. Design a half subtractor using only basic gates
4. Design a half adder using only basic gates
5. What is the function of a multiplexer select input?
6. How does encoder difference from decoder
7. Describe the application of multiplexer
8. What is the function of a decoder’s enable input(s)?
9. How does a priority encoder differ from an ordinary encoder
10. What is mean by magnitude comparator
11. What is demultiplexer? Explain the difference between a DEMUX and MUX
12. Define combinational logic circuit
13. What do you mean by propagation delay?
14. Write a short notes on one bit comparator
15. What will be the maximum number of outputs for a decoder with a 6 bit data word?
16. What is a data selector
17. Difference between decoder and encoder
18. What are the various modelling technique in HDL?
19. What is behavioural modelling?
20. What is data flow modelling?

# Part – C (12 marks)

* 1. Implement the following Boolean function with the help of 4:1 Mux. f(A,B,C,D) = ℿM(1,2,4,7,11,13,15).
  2. Implement the full subtractor with the help of 2:4 decoder.
  3. Implementation the full-subtractor using two half-subtractors.
  4. Show how a full order can be converted to a full subtractor with the addition of an inverter circuit.
  5. Describe the truth table of a subtractor and write the Boolean expression corresponding to the difference and borrow.
  6. Design a 4-bit Carry Look-Ahead Carry generator
  7. Design a binary adder as a subtractor with neat diagram
  8. Design a 8x4 PROM with 3 input and 4 output lines.
  9. implement the following function using PLA



* 1. Briefly explain 8 to 3 line encoder.
  2. Design 2:4 decoder and derive the boolean expression for output
  3. Design 4:1 mux with neat logic diagram
  4. Design 1:8 Demux with neat logic diagram